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Claims

[c1] 1.A method of forming a non-gated silicon on insulator diode in a semiconductor substrate, the substrate including a plurality of isolation regions formed therein, said method comprising:
forming a first structure on an upper surface of said substrate in a region between at least one pair of said isolation regions;
forming a first region of a first dopant type in said substrate, said first region comprising a first edge aligned to a first edge of said first structure; and
removing said first structure.

[c2] 2.The method of claim 1, further comprising forming a second region of a second dopant type in said substrate, the second region comprising a second edge aligned to a second edge of said first structure.

[c3] 3.The method of claim 1, further comprising forming a first silicide layer comprising a first silicide edge aligned to said first edge of said first structure.

[c4] 4.The method of claim 2, further comprising forming a second silicide layer comprising a second silicide edge

aligned to said second edge of said first structure.

[c5] 5.The method of claim 1, wherein said first structure comprises a hard mask.

[c6] 6.The method of claim 5, wherein said hard mask comprises a silicon nitride layer.

[c7] 7.The method of claim 1, wherein said first structure comprises a gate.

[c8] 8.The method of claim 7, wherein said first structure further comprises insulating spacers.

[c9] 9.The method of claim 8, wherein in said removing step, said spacers remain on said substrate.

[c10] 10.A method of forming a self-aligned SOI diode, said method comprising:
depositing a protective structure over a substrate;
implanting a plurality of diffusion regions of variable dopant types in an area between at least one pair of isolation regions in said substrate, said plurality of diffusion regions separated by a diode junction, wherein said implanting aligns an upper surface of said diode junction with said protective structure; and
removing said protective structure.

[c11] 11.The method of claim 10, further comprising forming

a silicide layer over said diffusion regions and aligned with said protective structure.

[c12] 12.The method of claim 10, wherein said protective structure comprises a hard mask.

[c13] 13.The method of claim 12, wherein said hard mask comprises a silicon nitride layer.

[c14] 14.The method of claim 10, wherein said protective structure comprises a polysilicon gate.

[c15] 15.The method of claim 14, wherein said protective structure further comprises insulating spacers.

[c16] 16.The method of claim 15, wherein in said removing step, said spacers remain on said substrate.

[c17] 17.A method of forming a self-aligned silicon over insulator diode, said method comprising:
implanting an N-well doping region in an implant region in between isolation regions in a semiconductor substrate;
configuring a gate over said implant region;
configuring a pair of sidewall spacers on sides of said gate;
using said gate to define P+ and N+ contact regions in said implant region;

removing said gate; and

using said sidewall spacers to align a silicide layer over said P+ and N+ contact regions.

[c18] 18.The method of claim 17, further comprising defining a diode junction region in between the P+ and N- regions and the N+ and N- regions.

[c19] 19.The method of claim 17, further comprising removing said sidewall spacers.

[c20] 20.The method of claim 17, further comprising depositing said silicide layer over said N-well doping region.